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Dated: February 5, 2010
Electronic Signature for Kevin J. Canning: /Kevin J. Canning/

Docket No.: MWS-039RCE
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Steve Johnson

Patent No.: 7636914 B1

Issued: December 22, 2009

For: SYSTEM AND METHOD FOR PROVIDING
CONTEXT TO OPERATOR OVERLOADING

**REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the Claims:

At column 9, line 2 (claim 10, line 2) of the printed patent, please insert --VHDL,-- before VERILOG.

At column 9, line 2 (claim 10, line 2) of the printed patent, please delete “Verilog” before C#.

At column 10, line 34 (claim 18, line 3) of the printed patent, please insert --objects-- before to.

At column 10, line 49 (claim 23, line 2) of the printed patent, please change “Verilog” to --VERILOG--.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: February 5, 2010

Respectfully submitted,

Electronic signature: /Kevin J. Canning/
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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7636914 B1
APPLICATION NO. : 10/692,524
ISSUE DATE : December 22, 2009
INVENTOR(S) : Steve JOHNSON

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 9, line 2 (claim 10, line 2) of the printed patent, please insert --VHDL,-- before VERILOG.

At column 9, line 2 (claim 10, line 2) of the printed patent, please delete "Verilog" before C#.

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Dated: February 5, 2010

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